

## Description

# [FLAT PANEL DISPLAY AND SOURCE DRIVER THEREOF]

### CROSS REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the priority benefit of Taiwan application serial no. 93102360, filed on February 03, 2004

### BACKGROUND OF INVENTION

[0002] Field of the Invention

[0003] This invention generally relates to a flat panel display, and more particularly to a source driver of a flat panel display.

[0004] Description of Related Art

[0005] A flat panel display (FPD) has the advantages of light weight, thin and compact size, and low power consumption. Hence it can occupy less space than traditional displays. Among several flat panel displays, the liquid crystal display (LCD) has the best chance to replace the traditional CRT monitors. To make more consumers replace traditional CRT monitors with LCD and enhance its com-

petitiveness, it is unavoidable to reduce its manufacture cost.

[0006] FIG. 1 is a block diagram of a conventional LCD. Referring to FIG. 1, the LCD panel 110 includes a plurality of gate channels 121 and source channels 131. The crossing of each gate channel and source channel has a pixel (not shown). The pixel status depends on the source channel signal 131 during the period that the gate channel signal 121 is on. The gate channel signals 121 are generated by the gate driver 120 based on the gate control signal G\_CONT. The source signals 131 are generated by the source driver 130 based on the clock signal CLK, display data DATA, and source control signal CONT. The gate control signal G\_CONT, the clock signal CLK, the display data DATA, and the source control signal CONT are provided by the timing controller 140.

[0007] To further describe the conventional source driver, a portion of the source driver of FIG. 1 is shown in FIGs. 1A and 1B. FIG. 1A shows a block diagram that a portion of the source driver is applied to a low-resistance circuit (e.g., FPC). Referring to FIG. 1A, due to the cost and the design flexibility, generally the source driver 130 will be implemented by combining several ICs (such as the source

drivers 130\_1–130\_n in FIG. 1A). Each IC provides a portion of the source channel signals 131. Each source driver IC generally is disposed on a flexible printer circuit board (FPC) so that the buses (CLK, DATA, CONT and other buses) between the timing controller 140 and the source drivers 130\_1–130\_n can transmit signals with a lower resistance.

[0008] However, the assembly cost for the FPC technology is too high to be acceptable and the yield rate is difficult to enhance. Hence, the number of the FPC has to be reduced. Hence, the conventional art disposes the source driver ICs on the LCD panel, and use ITO (indium tin oxide) to implement the circuit between the timing controller and the source drivers. FIG. 1B shows a block diagram that a portion of the source driver is applied to a high-resistance circuit (e.g., ITO). Referring to FIG. 1B, because ITO has a high resistance signal path, the equivalent resistors in FIG. 1B represent the resistance of the ITO signal paths. Therefore, the farther the source drivers 130\_1–130\_n are away from the timing controller 140, the larger the resistance between the source drivers 130\_1–130\_n and the timing controller 140. I.e., the higher resistance will reduce the max operation frequency of the system.

## SUMMARY OF INVENTION

- [0009] An object of the present invention is to provide a source driver suitable for a high resistance signal path (such as the ITO path in the LCD panel) in order to reduce the number of the FPC for connecting the timing controller and the LCD panel, and therefore to reduce the production cost. Further, the source driver of the present invention provides a transmitter to enhance the signal driving ability so as to overcome the high resistance of the signal path and increase the max operation frequency.
- [0010] Another object of the present invention is to provide a flat panel display by series-connecting the source drivers of the present invention so that the source driver in each stage enhances the signal driving ability and then sends it to the source driver in the next stage. Therefore, it can be used in a high resistance signal path (such as the ITO path in the LCD panel) in order to reduce the number of the FPC for connecting the timing controller and the LCD panel without sacrificing the performance, and therefore to reduce the production cost and increase the yield rate.
- [0011] Still another object of the present invention is to provide a source driver with options for setting the operation mode in a master mode or a slave mode in order to reduce

power consumption.

[0012] Still another object of the present invention is to provide the flat panel display that can set and adjust the source drive in each stage to be in a master mode or a slave mode based on the path resistance and the tolerance of the system delay time, in order to reduce the power consumption and the EMI.

[0013] The present invention provides a source driver, receiving a clock signal, a display data, and a control signal to drive a display panel, comprising: a receiver for receiving the clock signal, the display data, and the control signal; and a transmitter, coupled to the receiver, for enhancing a driving ability of the clock signal, the display data, and the control signal and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of another source driver in a next stage.

[0014] In a preferred embodiment of the present invention, the transmitter/receiver is a differential signal transmitter/receiver, or a TTL signal transmitter/receiver. The transmitter can also be a voltage mode signal transmitter or a current mode signal transmitter.

[0015] In a preferred embodiment of the present invention, the transmitter includes: a data synchronization circuit syn-

chronizing the clock signal, the display data, and the control signal received from the receiver; and a plurality of buffers, coupled to the data synchronization circuit, receiving the synchronized clock signal, the synchronized display data, and the synchronized control signal, enhancing the driving ability of the synchronized clock signal, the synchronized display data, and the synchronized control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage.

[0016] In a preferred embodiment of the present invention, the transmitter includes a plurality of voltage buffers receiving the clock signal, the display data, and the control signal, enhancing the driving ability of the clock signal, the display data, and the control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage.

[0017] The present invention provides a flat panel display, comprising: a display panel; a timing controller outputting a clock signal, a display data, and a control signal; and a plurality of source drivers, the plurality of source drivers being series-connected to be a series structure, the plu-

ality of source drivers being coupled to the display panel, one end of the series structure being coupled to the timing controller, the plurality of source drivers receiving the clock signal, the display data, and the control signal to drive the display panel, enhancing a driving ability of the clock signal, the display data, and the control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of another source driver in a next stage.

[0018] In a preferred embodiment of the present invention, each of the plurality of source drivers , comprises: a receiver for receiving the clock signal, the display data, and the control signal; and a transmitter, coupled to the receiver, for enhancing the driving ability of the clock signal, the display data, and the control signal and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage.

[0019] In a preferred embodiment of the present invention, the transmitter includes: a data synchronization circuit synchronizing the clock signal, the display data, and the control signal received from the receiver; and a plurality of buffers, coupled to the data synchronization circuit, re-

ceiving the synchronized clock signal, the synchronized display data, and the synchronized control signal, enhancing the driving ability of the synchronized clock signal, the synchronized display data, and the synchronized control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage.

[0020] In a preferred embodiment of the present invention, the transmitter includes a plurality of voltage buffers receiving the clock signal, the display data, and the control signal, enhancing the driving ability of the clock signal, the display data, and the control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage.

[0021] In a preferred embodiment of the present invention, the display panel is a  $\alpha$ -Si liquid crystal display panel or a low temperature poly-silicon liquid crystal display panel.

[0022] The present invention provides a source driver, receiving a master/slave setting signal, a clock signal, a display data, and a control signal to drive a display panel, comprising: a receiver for receiving the clock signal, the display data, and the control signal; and a transmitter, coupled to the



receiver, transmitter receiving the master/slave setting signal, the transmitter responsive to the master/slave setting signal operating in one of a master mode and a slave mode; wherein when the transmitter operates in the master mode, the transmitter enhances a driving ability of the clock signal, the display data, and the control signal and outputs the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of another source driver in a next stage; when the transmitter operates in the slave mode, the transmitter directly outputs the clock signal, the display data, and the control signal received from the receiver for use of the another source driver in the next stage.

[0023] In a preferred embodiment of the present invention, the transmitter/receiver is a differential signal transmitter/receiver, or a TTL signal transmitter/receiver. The transmitter can also be a voltage mode signal transmitter or a current mode signal transmitter.

[0024] The transmitter includes: a data synchronization circuit synchronizing the clock signal, the display data, and the control signal received from the receiver; and a plurality of buffers, coupled to the data synchronization circuit, receiving the synchronized clock signal, the synchronized

display data, and the synchronized control signal, enhancing the driving ability of the synchronized clock signal, the synchronized display data, and the synchronized control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage.

[0025] In a preferred embodiment of the present invention, the transmitter includes a plurality of voltage buffers receiving the clock signal, the display data, and the control signal, enhancing the driving ability of the clock signal, the display data, and the control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage.

[0026] The present invention provides A flat panel display, comprising: a display panel; a timing controller outputting a clock signal, a display data, and a control signal; a control circuit outputting a plurality of master/slave setting signals; and a plurality of source drivers, the plurality of source drivers being series-connected to be a series structure, the plurality of source drivers being coupled to the display panel, one end of the series structure being coupled to the timing controller, the plurality of source

drivers receiving the clock signal, the display data, and the control signal to drive the display panel, each of the plurality of source drivers responsive to a corresponding one of the plurality of master/slave setting signals determining whether to enhancing a driving ability of the clock signal, the display data, and the control signal, and outputting the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of another source driver in a next stage.

[0027] In a preferred embodiment of the present invention, each of the plurality of source drivers , comprises: a receiver for receiving the clock signal, the display data, and the control signal; and a transmitter, coupled to the receiver, transmitter receiving the master/slave setting signal, the transmitter responsive to the master/slave setting signal operating in one of a master mode and a slave mode; wherein when the transmitter operates in the master mode, the transmitter enhances the driving ability of the clock signal, the display data, and the control signal and outputs the enhanced clock signal, the enhanced display data, and the enhanced control signal for use of the another source driver in the next stage; when the transmitter operates in the slave mode, the transmitter directly out-

puts the clock signal, the display data, and the control signal received from the receiver for use of the another source driver in the next stage.

[0028] In a preferred embodiment of the present invention, the display panel is  $\alpha\alpha$ -Si liquid crystal display panel or a low temperature poly-silicon liquid crystal display panel.

[0029] The present invention utilizes the series connection structure to couple the source drivers and enhances the driving ability of the received clock signal, display data, and the control signal. Hence, the present invention can be applied to a high resistance path (such as the ITO path in the LCD panel) in order to reduce the number of the FPC for connecting the timing controller and the LCD panel without sacrificing the performance so as to overcome the high resistance of the signal path and increase the max operation frequency. Therefore, the present invention can reduce the production cost and increase the yield rate.

[0030] The present invention further provides the option to set the source driver in a master mode or a slave mode based on the path resistance and the tolerance of the system delay time, in order to reduce the power consumption and the EMI.

[0031] The above is a brief description of some deficiencies in

the prior art and advantages of the present invention. Other features, advantages and embodiments of the invention will be apparent to those skilled in the art from the following description, accompanying drawings and appended claims.

#### **BRIEF DESCRIPTION OF DRAWINGS**

- [0032] FIG. 1 is a block diagram of a conventional LCD.
- [0033] FIG. 1A shows a block diagram that a portion of the source driver in FIG. 1 is applied to a low-resistance circuit (e.g., FPC).
- [0034] FIG. 1B shows a block diagram that a portion of the source driver in FIG. 1 is applied to a high-resistance circuit (e.g., ITO).
- [0035] FIG. 2 is a block diagram of a LCD in accordance with a preferred embodiment of the present invention.
- [0036] FIG. 2A shows a block diagram of a portion of the source driver in FIG. 2 FIG. 2B is a block diagram of a source driver in FIG.2 in accordance with a preferred embodiment of the present invention.
- [0037] FIG. 2C is a timing sequence of the after-synchronized input data of the source driver of FIG. 2B.
- [0038] FIG. 2D is another block diagram of a source driver in

FIG.2 in accordance with a preferred embodiment of the present invention.

[0039] FIG. 3A a block diagram of a display source drive circuit in accordance with another preferred embodiment of the present invention.

[0040] FIG. 3B a block diagram of a source driver (in a slave mode) in accordance with another preferred embodiment of the present invention.

[0041] FIG. 3C a block diagram of a source driver (in a master mode) in accordance with another preferred embodiment of the present invention.

[0042] FIG. 3D a block diagram of another source driver (in a master mode) in accordance with another preferred embodiment of the present invention.

#### **DETAILED DESCRIPTION**

[0043] To facilitating illustration of the present invention, the following embodiments use LCD as an example. It should be noted that the present invention is not limited to LCD.

[0044] FIG. 2 is a block diagram of a LCD in accordance with a preferred embodiment of the present invention. Referring to FIG. 2, there are a plurality of gate channels 221 and source channels 231 cross-disposed on the LCD panel 210. The crossing of each gate channel and source chan-

nel has a pixel (not shown). The pixel status depends on the source channel signal 231 during the period that the gate channel signal 221 is on. The gate channel signals 221 are generated by the gate driver 220 based on the gate control signal G\_CONT. The source signals 231 are generated by the source driver 230 based on the clock signal CLK, display data DATA, and source control signal CONT. The gate control signal G\_CONT, the clock signal CLK, the display data DATA, and the source control signal CONT are provided by the timing controller 240.

[0045] To further describe the source driver in accordance of a preferred embodiment, a portion of the source driver of FIG. 2 is shown in FIG. 2A. FIG. 2A shows a block diagram of a portion of the source driver in FIG. 2. Referring to FIG. 2A, the source drivers 230\_1–230\_n are series-connected to be a series structure. One end of the series structure (in this embodiment it is the source driver 230\_1) is coupled to the timing controller 240. The source drivers 230\_1–230\_n respectively provide a portion of the source channel signal 231. The equivalent resistor R in FIG. 2A represents the resistance of the signal path such as the ITO path on the display panel. The source drivers receive the clock signal CLK, the display data DATA, and the con-

trol signal CONT to drive the display panel (such as the LCD panel 210 in FIG. 2), enhance the driving ability of the clock signal CLK, the display data DATA, and the control signal CONT, and then output those signals for the use of the source driver in the next stage.

[0046] The source driver in the above embodiment can be implemented as shown in FIG. 2B. FIG. 2B is a block diagram of a source driver in FIG.2 in accordance with a preferred embodiment of the present invention. Referring to FIG. 2B, the receiver 250 of the source driver 230 receives the clock signal CLK, the display data DATA, and the control signal CONT from the timing controller 240 or the source driver in the previous stage. The channel driving circuit 260 obtains the clock signal CLK, the display data DATA, and the control signal CONT from the receiver 250 and based on those signals generates a plurality of source channel signals 231. Each source channel signal 231 will drive the corresponding source channel. The receiver 250 and the channel driving circuit 260 can be implemented by prior art and is not necessary to describe it here.

[0047] The transmitter 270 in this embodiment includes the data synchronization circuit 271 and the buffers 272. The data synchronization circuit 271 receives a plurality of signals,



synchronizes those signals, and outputs the synchronized signals. In this embodiment, for example, the clock signal CLK can be used as a base for synchronizing the other signals. The buffers 272 respectively receive the clock signal CLK, the display data DATA, and the control signal CONT, enhance their driving ability, and then output those enhanced clock signal OCLK, the display data ODATA, and the control signal OCONT.

[0048] FIG. 2C is a timing sequence of the after-synchronized input data of the source driver of FIG. 2B. Referring to FIGs. 2B and 2C, assuming that the display data DATA has two data lines DATA<sub>x</sub> and DATA<sub>y</sub>, because the equivalent resistance and the stray capacitance of the signal transmission paths for data lines DATA<sub>x</sub> and DATA<sub>y</sub> is different, the transmission delay will be different. As shown in FIG. 2C, the data lines DATA<sub>x</sub> and DATA<sub>y</sub> will have a path delay T<sub>skew</sub>. After through the data synchronization circuit 271 and the buffers 272, the path delay T<sub>skew</sub> between the signals will be compensated. Hence, the transmission delay will not accumulated. As shown in FIG. 2C, the data ODATA<sub>x</sub> and ODATA<sub>y</sub> will be sent out at the same time for the use of the source driver in the next stage.

[0049] In this embodiment, the signals transmitted between the source drivers for example are voltage mode differential signals, current mode differential signals, TTL signals, or other types of signals.

[0050] The source driver in the above embodiment can be implemented as shown in FIG. 2D. FIG. 2D is another block diagram of a source driver in FIG.2 in accordance with a preferred embodiment of the present invention. Referring to FIG. 2D, the receiver and the transmitter can be implemented by a plurality of voltage buffers 280. The source driver 230 receives the clock signal CLK, the display data DATA, and the control signal CONT from the timing controller 240 or the source driver in the previous stage. The channel driving circuit 260 obtains the clock signal CLK, the display data DATA, and the control signal CONT and based on those signals generates a plurality of source channel signals 231. Each source channel signal 231 will drive the corresponding source channel. The voltage buffers 280 respectively receive the clock signal CLK, the display data DATA, and the control signal CONT, enhance their driving ability and then output those enhanced clock signal OCLK, the display data ODATA, and the control signal OCONT.

[0051] Hence, this embodiment can apply the source driver in a high resistance circuit such as ITO without sacrificing the performance. In addition, because the source driver is disposed on the display panel, it can reduce the number of the FPC and thus reduce the assembly cost of the flat panel display and enhance the yield rate.

[0052] To reduce the power consumption, if the signal path delay is in an acceptable range, the present invention provides a bus structure which uses a transmitter to drive a plurality of source drivers. FIG. 3A a block diagram of a display source drive circuit in accordance with another preferred embodiment of the present invention. Referring to FIG. 3A, the source drivers 330\_1–330\_n are series-connected to be a series structure. One end of the series structure (in this embodiment it is the source driver 330\_1) is coupled to the timing controller 340. The source drivers 330\_1–330\_n respectively provide a portion of the source channel signal 331. The equivalent resistor R in FIG. 3A represents the resistance of the signal path such as the ITO path on the display panel. The source drivers receive the clock signal CLK, the display data DATA, and the control signal CONT to drive the display panel (such as the LCD panel 210 in FIG. 2).

[0053] The source drivers 330\_1–330\_n respectively receive the master/slave setting signals M\_S\_1 M\_S\_n. The source drivers based on the master/slave setting signals operate in one of the master mode or the slave mode. When the source driver operates in the master mode, it will enhance the driving ability of the clock signal CLK, the display data DATA, and the control signal CONT, and then output those signals for the use of the source driver in the next stage. When the source driver operates in the slave mode, the source driver will directly output the clock signal CLK, the display data DATA, and the control signal CONT in order to reduce power consumption. The master/slave setting signals M\_S\_1 M\_S\_n are provided by the control circuit 390.

[0054] FIG. 3B a block diagram of a source driver (in a slave mode) in accordance with another preferred embodiment of the present invention. Referring to FIG. 3B, the source driver 330 receives the clock signal CLK, the display data DATA, and the control signal CONT from the timing controller 340 or the source driver in the previous stage. The channel driving circuit 360 obtains the clock signal CLK, the display data DATA, and the control signal CONT and based on those signals generates a plurality of source

channel signals 331. Each source channel signal 331 will drive the corresponding source channel. The source driver 330 further receives the master/slave setting signal M\_S. For example, when the master/slave setting signal M\_S is low, the source driver 330 is set to operate in the slave mode; when the master/slave setting signal M\_S is high, the source driver 330 is set to operate in the master mode. When the source driver operates in the slave mode, the source driver will directly output the clock signal CLK, the display data DATA, and the control signal CONT via the pass line.

[0055] When the master/slave setting signal M\_S is high, the source driver 330 is set to operate in the master mode. FIG. 3C a block diagram of a source driver (in a master mode) in accordance with another preferred embodiment of the present invention. Referring to FIG. 3C, the source driver 330 includes a receiver 350 and a transmitter 370. In this embodiment, when the source driver 330 is set to operate in the master mode, the operation is similar to the previous embodiment shown in FIG. 2B and thus is not necessary to describe again.

[0056] FIG. 3D a block diagram of another source driver (in a master mode) in accordance with another preferred em-

bodiment of the present invention. Referring to FIG. 3D, the receiver and the transmitter are implemented by a plurality of voltage buffers 380. The operation of the embodiment in FIG. 3D is similar to the previous embodiment shown in FIG. 2D and thus is not necessary to describe again.

[0057] In this embodiment, the operation mode of each source drivers flexibly depends on the range of the acceptable system time delay. Taking a LCD panel with ten source drivers as an example, the possible combination of the source drivers can be M-M-M-M-M-M-M-M-M-M, M-S-M-S-M-S-M-S-M-S, M-S-S-M-S-S-M-S-S-S, M-S-S-S-M-S-S-S-M-S, or M-S-S-S-S-M-S-S-S-S; wherein M represents that the source driver operates in the master mode and S represents that the source driver operates in the slave mode. The above combination of the source drivers can be adjusted based on the resistance of the signal path. Hence, this embodiment can further reduce the power consumption and EMI.

[0058] The above description provides a full and complete description of the preferred embodiments of the present invention. Various modifications, alternate construction, and equivalent may be made by those skilled in the art without

changing the scope or spirit of the invention. Accordingly, the above description and illustrations should not be construed as limiting the scope of the invention which is defined by the following claims.